Wide V_{IN} Range Fault Protected 50mA Step-Down Charge Pump

FEATURES

- **Input Voltage Range: 4V to 48V**
- **Adjustable Regulated Output: 2.4V to 12.5V**
- **Output Current: 50mA Maximum**
- **16µA Quiescent Current in Regulation at No Load**
- **Input Fault Protection from –52V to 60V**
- **Multimode Charge Pump (2:1, 1:1) with Automatic Mode Switching Maintains Regulation Over Wide V_{IN} Range**
- **Input Voltage Shunt Mode for Current-Fed Applications**
- Power Good Output
- Overtemperature and Short-Circuit Protection
- Operating Junction Temperature: 150°C Maximum
- Thermally Enhanced 10-Lead MSOP and 10-Lead (3mm × 3mm) DFN packages

APPLICATIONS

- Industrial Control, Factory Automation, Sensors, and SCADA Systems
- Housekeeping Power Supplies
- Current-Boosting Voltage Regulators for 4mA to 20mA Current Loops

DESCRIPTION

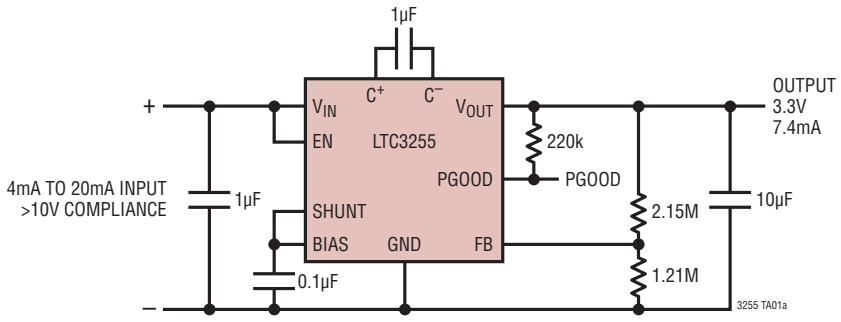
The LTC®3255 is a switched-capacitor step-down DC/DC converter that produces a regulated output (2.4V to 12.5V adjustable) from a 4V to 48V input. In applications where the input voltage exceeds twice the output voltage, 2:1 capacitive charge pumping extends output current capability beyond input supply current limits. At no load, Burst Mode® operation cuts V_{IN} quiescent current to 16µA.

With its integrated V_{IN} shunt regulator, the LTC3255 excels in 4mA to 20mA current loop applications. The device enables current multiplication; a 4mA input current can power a 7.4mA load continuously. Alternatively, the LTC3255 serves as a higher efficiency replacement for linear regulators and provides a space-saving inductor-free alternative to buck DC/DC converters.

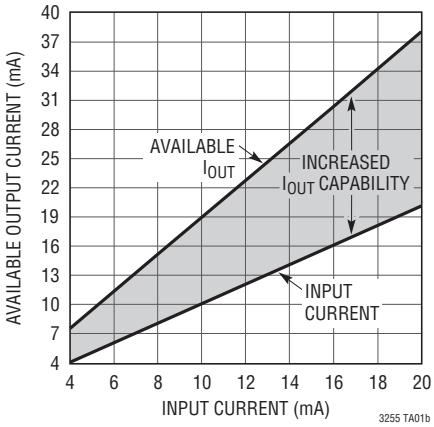
The LTC3255 withstands reverse-polarity input supplies and output short-circuits without damage. Safety features including current limit and overtemperature protection further enhance robustness. The LTC3255 is available in thermally enhanced 10-lead MSOP and low profile 3mm × 3mm 10-lead DFN packages.

TYPICAL APPLICATION

7.4mA DC Supply from 4mA to 20mA Current Loop



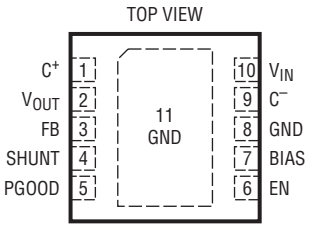
Available Output Current vs Input Current



ABSOLUTE MAXIMUM RATINGS (Notes 1, 2)

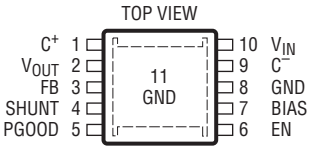
V_{IN}, EN ..... –52V to 60V
V_{OUT} 15V
V_{OUT} Short-Circuit Duration (Note 6) ..... Indefinite
I_{VOUT} When V_{OUT} < 0V (Note 4) 50mA
FB ..... ±6V
PGOOD 15V
I_{PGOOD} When V_{PGOOD} < 0V (Note 5) 100µA
Operating Junction Temperature
Range (Notes 3, 6) ..... –55°C to 150°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec)
MSE Only ..... 300°C

PIN CONFIGURATION



DD PACKAGE
10-LEAD (3mm × 3mm) PLASTIC DFN

T_{JMAX} = 150°C, θ_{JA} = 43°C/W
EXPOSED PAD (PIN 11) IS GND, MUST BE SOLDERED TO PCB



MSE PACKAGE
10-LEAD PLASTIC MSOP

T_{JMAX} = 150°C, θ_{JA} = 40°C/W
EXPOSED PAD (PIN 11) IS GND, MUST BE SOLDERED TO PCB

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC3255EDD#PBF	LTC3255EDD#TRPBF	LGHD	10-Lead (3mm × 3mm) Plastic DFN	–40°C to 125°C
LTC3255IDD#PBF	LTC3255IDD#TRPBF	LGHD	10-Lead (3mm × 3mm) Plastic DFN	–40°C to 125°C
LTC3255HDD#PBF	LTC3255HDD#TRPBF	LGHD	10-Lead (3mm × 3mm) Plastic DFN	–40°C to 150°C
LTC3255MPDD#PBF	LTC3255MPDD#TRPBF	LGHD	10-Lead (3mm × 3mm) Plastic DFN	–55°C to 150°C
LTC3255EMSE#PBF	LTC3255EMSE#TRPBF	LTGHF	10-Lead Plastic MSOP	–40°C to 125°C
LTC3255IMSE#PBF	LTC3255IMSE#TRPBF	LTGHF	10-Lead Plastic MSOP	–40°C to 125°C
LTC3255HMSE#PBF	LTC3255HMSE#TRPBF	LTGHF	10-Lead Plastic MSOP	–40°C to 150°C
LTC3255MPMSE#PBF	LTC3255MPMSE#TRPBF	LTGHF	10-Lead Plastic MSOP	–55°C to 150°C

Consult LTC Marketing for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.
Consult LTC Marketing for information on nonstandard lead based finish parts.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the specified operating junction temperature range, otherwise specifications are at T_A = 25°C. V_{IN} = 12V unless otherwise noted. (Notes 2, 3)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{IN}	Input Voltage Range (Note 7)		●	4		48	V
V_{OUT}	Output Voltage Range		●	2.4		12.5	V
V_{UVLO_BK}	V_{IN} Undervoltage Lockout Threshold with Shunt Disabled	V_{IN} Rising, SHUNT = GND Hysteresis, SHUNT = GND			2.4 50	2.7	V mV
V_{UVLO_SH}	V_{IN} Undervoltage Lockout Threshold with Shunt Enabled	V_{IN} Rising, SHUNT= BIAS Hysteresis, SHUNT= BIAS			5 200	5.7	V mV
I_{VIN}	V_{IN} Quiescent Current EN Low EN High, SHUNT = GND EN High, SHUNT = BIAS	 Shutdown Enabled, Output in Regulation Enabled, Output in Regulation			 3 16 30	 6 35 45	 µA µA µA
I_{VOUT}	Available Output Current Shunt Disabled Shunt Enabled	 SHUNT = GND SHUNT = BIAS, I_{VIN} = 4mA, V_{OUT} = 3.3V	 ● ●	 50 7.4	 7.8	 	 mA mA
V_{FB}	Regulated Feedback Voltage		●	1.176	1.200	1.224	V
I_{FB}	FB Pin Leakage	V_{FB} = 1.3V				±10	nA
V_{EN_VIH}	EN High Level Input Voltage		●	1.4			V
V_{EN_VIL}	EN Low Level Input Voltage		●			0.4	V
I_{EN}	EN Pin Input Current	V_{EN} = 12V V_{EN} = 0V			0 0	±1 ±1	µA µA
I_{LIM}	V_{OUT} Current Limit				120		mA
f_{OSC}	Oscillator Frequency				500		kHz
$V_{PGTHRESH}$	PGOOD Rising Threshold	% of Final Regulation Voltage	●	90	94	98	%
$V_{PG(LOW)}$	PGOOD Output Low Voltage	I_{PGOOD} = 200µA			0.1	0.4	V
	PGOOD High Impedance Leakage	V_{PGOOD} = 12V	●			1	µA

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: All voltages are referenced to GND unless otherwise specified.

Note 3: The LTC3255E is guaranteed to meet performance specifications from 0°C to 85°C operating junction temperature. Specifications over the –40°C to 125°C operating junction temperature range are assured by design, characterization and correlation with statistical process controls. The LTC3255I is guaranteed over the –40°C to 125°C operating junction temperature range. The LTC3255H is guaranteed over the –40°C to 150°C operating junction temperature range. The LTC3255MP is guaranteed over the –55°C to 150°C operating junction temperature range. High junction temperatures degrade operating lifetimes; operating lifetime is derated for junction temperatures greater than 125°C. Note that the maximum ambient temperature consistent with these specifications is determined by specific operating conditions in conjunction with board layout, the rated package thermal resistance and other environmental factors.

The junction temperature (T_J, in °C) is calculated from the ambient temperature (T_A, in °C) and power dissipation (P_D, in Watts) according to the formula:

$$T_J = T_A + (P_D \bullet \theta_{JA})$$

where θ_{JA} (in °C/W) is the package thermal impedance.

Note 4: The LTC3255 has an internal diode that conducts whenever V_{OUT} is pulled below GND. When so pulled, absolute maximum current out of V_{OUT} is 50mA.

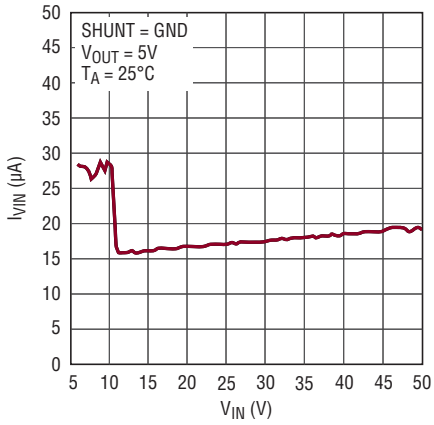
Note 5: The LTC3255 has an internal diode that conducts whenever PGOOD is pulled below GND. When so pulled, absolute maximum current out of PGOOD is 100µA.

Note 6: This IC has overtemperature protection that is intended to protect the device during momentary overload conditions. Junction temperatures will exceed 150°C when overtemperature protection is active. Continuous operation above the specified maximum operating junction temperature may impair device reliability.

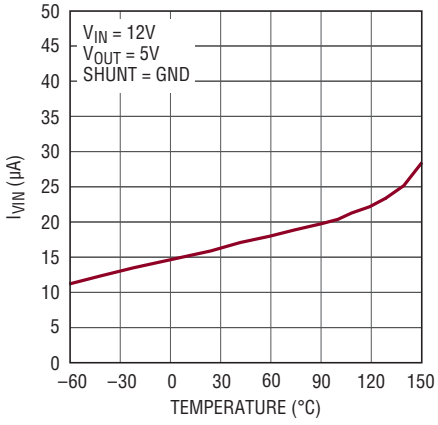
Note 7: This IC has input overvoltage protection that shuts down the device whenever V_{IN} exceeds the specified input voltage range. Shutdown typically occurs when V_{IN} exceeds 52V. V_{IN} subsequently must fall below 50V (typical) for the IC to re-enable.

TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C, unless otherwise noted.

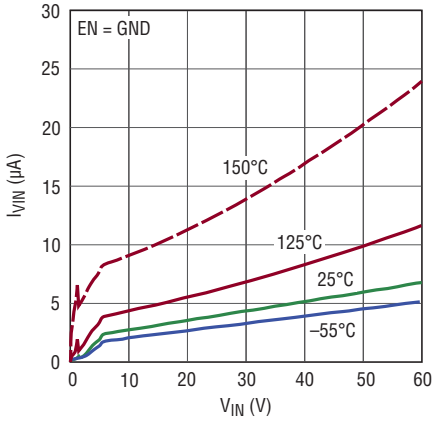
Input Operating Current vs Input Voltage



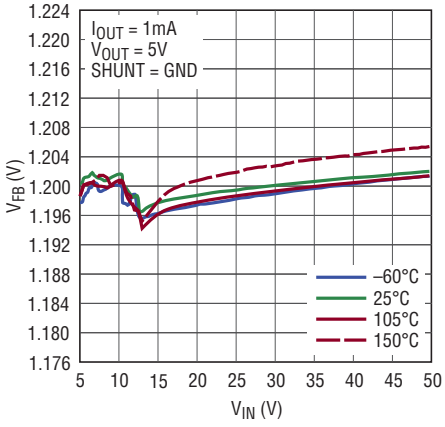
Input Operating Current vs Temperature



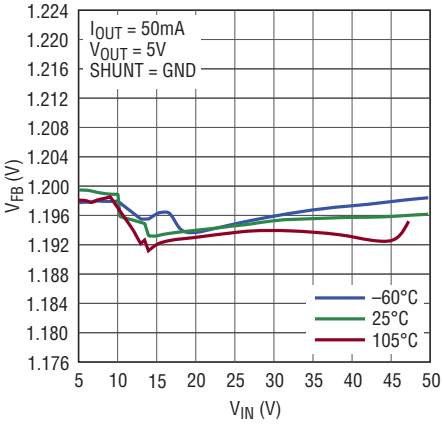
Input Shutdown Current vs Input Voltage



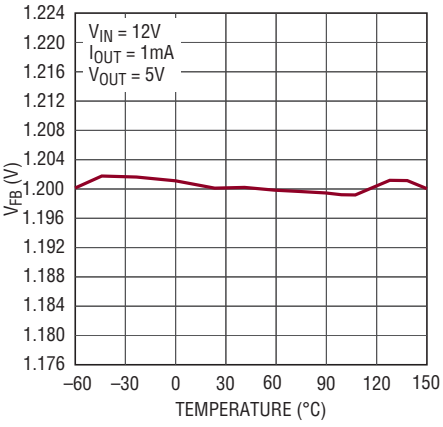
FB Pin Regulation Voltage vs Input Voltage (I_{OUT} = 1mA)



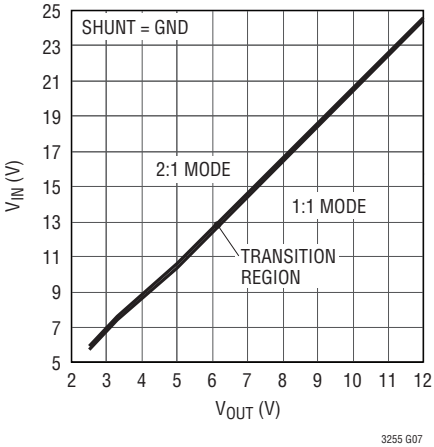
FB Pin Regulation Voltage vs Input Voltage (I_{OUT} = 50mA)



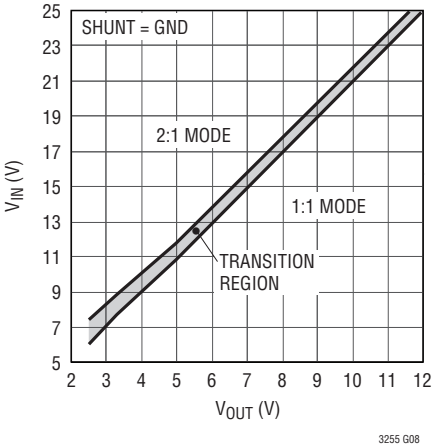
FB Pin Regulation Voltage vs Temperature



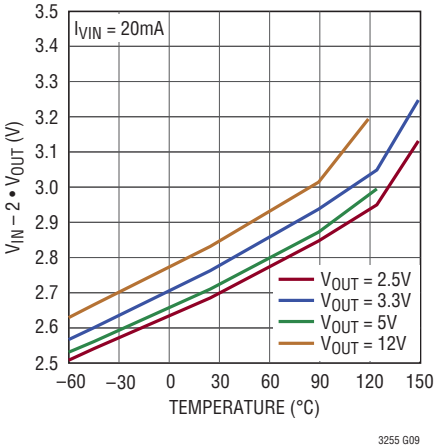
Operating Mode Transition Voltage vs Input Voltage (I_{OUT} = 5mA)



Operating Mode Transition Voltage vs Input Voltage (I_{OUT} = 50mA)

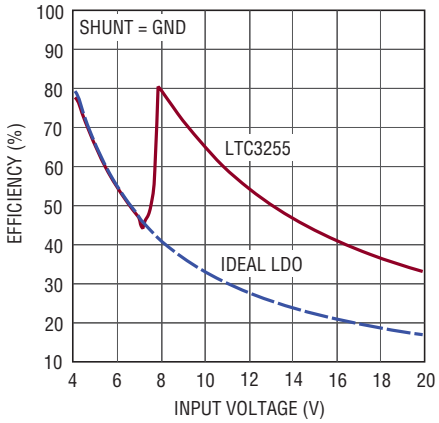


Typical Minimum $V_{IN} – 2 • V_{OUT}$ Compliance Required for Shunt Mode Operation

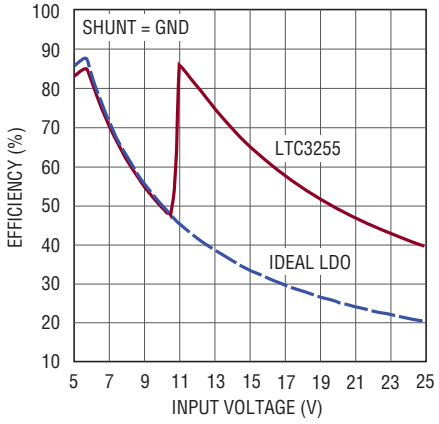


TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C, unless otherwise noted.

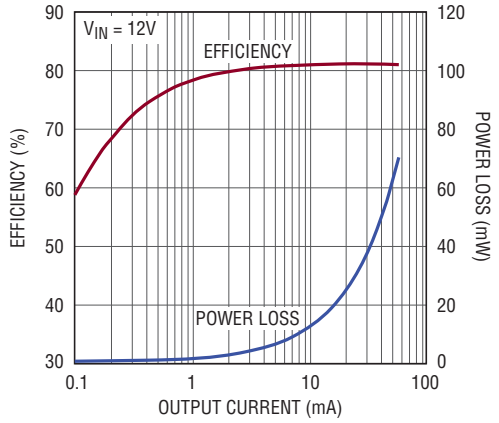
3.3V_{OUT} Efficiency vs Input Voltage at 50mA Load



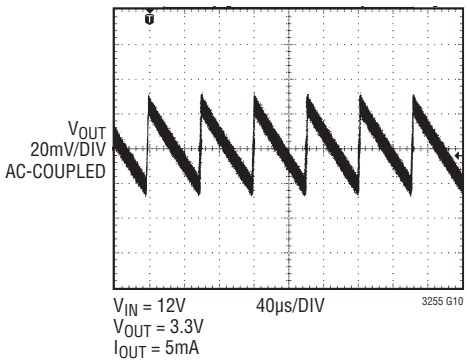
5V_{OUT} Efficiency vs Input Voltage at 50mA Load



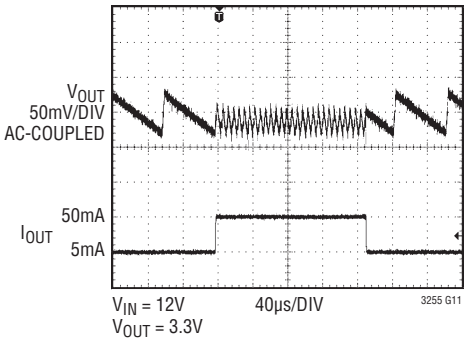
5V_{OUT} Efficiency vs Output Current



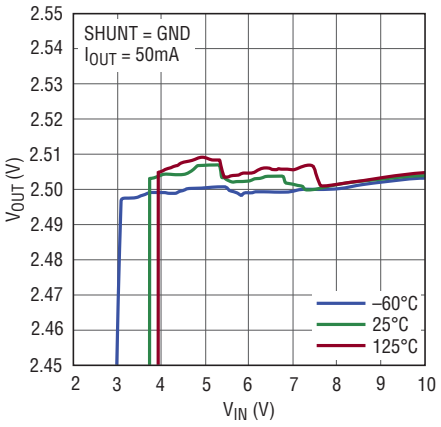
Output Ripple



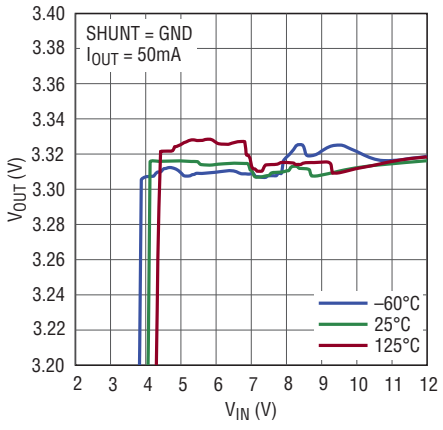
Load Transient



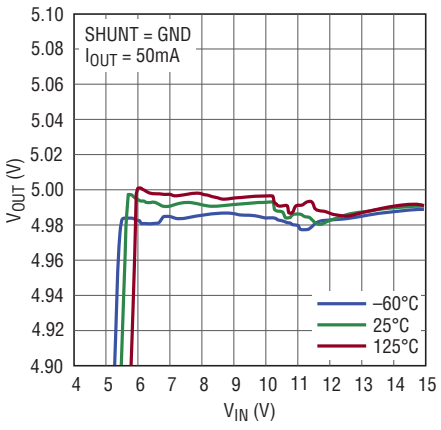
2.5V Output Voltage vs Falling Input Voltage



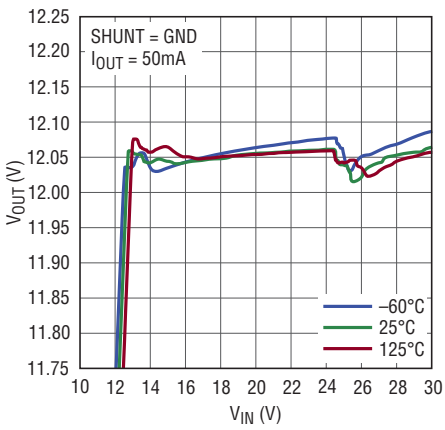
3.3V Output Voltage vs Falling Input Voltage



5V Output Voltage vs Falling Input Voltage



12V Output Voltage vs Falling Input Voltage



PIN FUNCTIONS

C^+ (Pin 1): Flying Capacitor Positive Connection. This pin must not be driven externally.

V_{OUT} (Pin 2): Charge Pump Output Voltage.

FB (Pin 3): Feedback pin for setting the regulated output voltage, usually connected to V_{OUT} through an external resistor divider. In operation, the LTC3255 servos the FB pin to 1.2V by transferring charge from V_{IN} to V_{OUT}.

SHUNT (Pin 4): Configuration pin that must connect to either the BIAS or GND pins to enable or defeat, respectively, the LTC3255's shunt regulator feature. Connect this pin to either BIAS or GND on the circuit board layout. Do not float this pin.

PGOOD (Pin 5): Power Good Open-Drain Logic Output. This pin becomes high impedance when the feedback voltage on the FB pin rises above 94% (typical) of the regulation voltage.

EN (Pin 6): Logic Input. A logic high on the EN pin will enable the charge pump. A logic low shuts down the LTC3255. Do not float this pin.

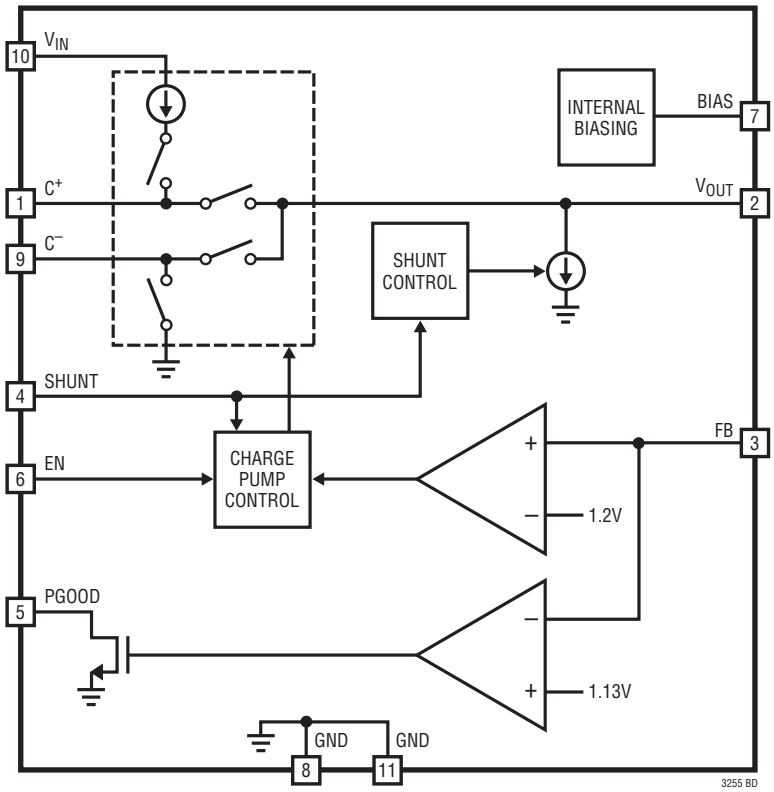
BIAS (Pin 7): Connect this pin to a 0.1µF bypass capacitor to GND. A ceramic capacitor of at least 10V rating is recommended.

GND (Pin 8 and Exposed Pad Pin 11): Ground Connection. Exposed pad (Pin 11) must be soldered to the circuit board ground plane for proper thermal and electrical conduction.

C^- (Pin 9): Flying Capacitor Negative Connection. This pin must not be driven externally.

V_{IN} (Pin 10): Input Supply Voltage. Bypass this pin to GND with at least 1µF capacitance.

SIMPLIFIED BLOCK DIAGRAM



APPLICATIONS INFORMATION

General Operation

The LTC3255 uses switched-capacitor-based DC/DC conversion to provide efficiency advantages associated with inductor-based circuits together with the cost and simplicity advantages of linear regulators. No inductors are required. The LTC3255 uses an internal switch network and fractional conversion ratios to achieve high efficiency and regulation over widely varying V_{IN} and output load conditions. A defeatable V_{IN} shunt regulator allows the LTC3255 to operate with current-fed V_{IN} supplies, such as 4mA to 20mA current loops.

Automatic 2:1/1:1 Mode Switching with V_{IN} Shunt Disabled (SHUNT Pin Connected to GND)

Connecting the SHUNT pin to GND defeats the V_{IN} shunt regulator. With the shunt regulator defeated, the LTC3255 functions as a general purpose step-down charge pump offering two conversion modes: 2:1 and 1:1. Internal circuitry automatically chooses the optimal conversion ratio based on V_{IN}, V_{OUT}, and output load conditions, generally preferring 2:1 mode when V_{IN} exceeds twice V_{OUT}, but falling back to 1:1 mode as needed to maintain regulation.

Forced 2:1 Mode Operation When V_{IN} Shunt Regulator is Enabled (SHUNT Pin Connected to BIAS)

With the SHUNT pin connected to BIAS, the V_{IN} shunt regulator is enabled, and the LTC3255 expects a high impedance power source at V_{IN}, such as a 4mA to 20mA current loop, or a resistor to a DC supply. With the shunt regulator enabled, the charge pump runs in 2:1 conversion mode only, extending its output current capability beyond that of the V_{IN} source. For example, the LTC3255 can typically boost the current capability of a 4mA source to power a 7.4mA load continuously. See V_{IN} Shunt Regulator in the Operation section for V_{IN} compliance and other operating information.

Regulation Loop

Regulation is achieved via a Burst Mode control loop that allows the LTC3255 to achieve high efficiency even at light loads. As shown in the Block Diagram, a comparator monitors the output voltage via a feedback pin, FB, which receives a fraction of V_{OUT} via an external resistor divider. While V_{FB} is below regulation, the LTC3255 transfers fixed packets of charge from V_{IN} to V_{OUT}, paced by an internal oscillator. This causes V_{OUT} and hence FB to rise. When V_{FB} enters regulation, the LTC3255 stops charge transfer and enters a low quiescent current sleep state. During this sleep state, the output load is supplied entirely by the output capacitor. The LTC3255 remains in sleep until the output drops enough to require another burst of charge. As load current decreases, the output capacitor takes longer to discharge, so sleep time increases.

Shutdown and Undervoltage Lockout (UVLO)

Driving the EN pin low puts the LTC3255 in shutdown, which disables all circuitry except the internal bias. V_{IN} supply current is minimized. When the EN pin is high, the charge pump will enable if V_{IN} satisfies the V_{IN} undervoltage lockout (UVLO) threshold. If the shutdown feature is not needed, the EN pin can be connected to V_{IN}, as both pins share the same Absolute Maximum rating.

Reverse Polarity Input Protection

The V_{IN} and EN pins are designed to withstand connection to voltages below ground without damage. When V_{IN} is below ground, the LTC3255 prevents V_{OUT} from going more than a diode drop below GND to protect the load circuit.

Short-Circuit/Thermal Protection

The LTC3255 has built-in short-circuit current limiting as well as overtemperature protection. During short-circuit conditions output current is automatically limited by the output current limit circuitry.

APPLICATIONS INFORMATION

The LTC3255 has thermal protection that will shut down the device if the junction temperature exceeds the overtemperature threshold (typically 175°C). Thermal shutdown is included to protect the IC in cases of excessively high ambient temperatures, or in cases of excessive power dissipation inside the IC. The charge transfer will reactivate once the junction temperature drops back to approximately 165°C.

When the thermal protection is active, the junction temperature is beyond the specified operating range. Thermal protection is intended for momentary overload conditions outside normal operation. Continuous operation above the specified maximum operating junction temperature may impair device reliability.

Programming the Output Voltage (FB Pin)

The LTC3255 output voltage is set by connecting its FB pin to a resistor divider between V_{OUT} and GND as shown in Figure 1.

The desired adjustable output voltage is programmed by solving the following equation for R_A and R_B:

$$\frac{R_A}{R_B} = \frac{V_{OUT}}{1.2V} - 1$$

Select a value for R_B in the range of 20k to 2M and solve for R_A. Note that the resistor divider current adds to the total no-load operating current. Thus a larger value for R_B will result in lower operating current.

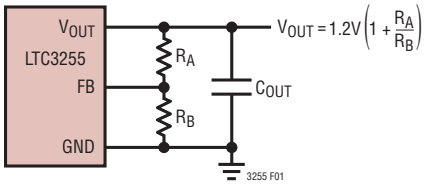


Figure 1. Setting the Output Voltage

2:1 Step-Down Charge Pump Operation

In 2:1 step-down mode, charge transfer from V_{IN} to V_{OUT} happens in two phases. On the first phase, the flying capacitor (C_{FLY}) is connected between V_{IN} and V_{OUT}. On this phase C_{FLY} is charged up and current is delivered to V_{OUT}. On the second phase, C_{FLY} is connected between V_{OUT} and GND. The charge stored on C_{FLY} during the first phase is transferred to V_{OUT} on the second phase. When in 2:1 step-down mode, the input current will be approximately half of the total output current. The efficiency (η) and chip power dissipation (P_D) in 2:1 mode are approximately:

$$\eta = \frac{P_{OUT}}{P_{IN}} = \frac{V_{OUT} \bullet I_{OUT}}{V_{IN} \bullet \frac{1}{2} I_{OUT}} = \frac{2V_{OUT}}{V_{IN}}$$

$$P_D = \left(\frac{V_{IN}}{2} - V_{OUT} \right) I_{OUT}$$

1:1 Step-Down Charge Pump Operation

1:1 step-down mode is similar to how a linear regulator works. Charge is delivered directly from V_{IN} to V_{OUT} through most of the internal oscillator period. The charge transfer is briefly interrupted at the end of the period. When in 1:1 step-down mode the input current will be approximately equal to the total output current. Thus efficiency (η) and chip power dissipation (P_D) in 1:1 mode are approximately:

$$\eta = \frac{P_{OUT}}{P_{IN}} = \frac{V_{OUT} \bullet I_{OUT}}{V_{IN} \bullet I_{OUT}} = \frac{V_{OUT}}{V_{IN}}$$

$$P_D = (V_{IN} - V_{OUT}) I_{OUT}$$

APPLICATIONS INFORMATION

Power Good Output Operation (PGOOD)

The LTC3255 includes an open-drain power good (PGOOD) output pin. If the chip is in shutdown or undervoltage lockout, or if the FB pin voltage is less than 90% (typical) of its regulation voltage, PGOOD is low impedance to ground. PGOOD becomes high impedance when V_{OUT} rises to 94% (typical) of its regulation voltage. PGOOD stays high impedance until V_{OUT} is shut down or drops below the PGOOD falling threshold (90% typical). A pull-up resistor can be inserted between PGOOD and V_{OUT} to signal a valid power good condition. The use of a large value pull-up resistor on PGOOD and a capacitor placed between PGOOD and GND can be used to delay the PGOOD signal if desired.

V_{IN} Shunt Regulator Operation

The V_{IN} shunt regulator feature of the LTC3255 is intended for applications where V_{IN} is current-fed, such as in 4mA to 20mA current loops. A circuit powered by a current loop must limit the voltage drop it presents to the loop to avoid exceeding the loop compliance, which would break the current loop. The LTC3255's V_{IN} shunt regulator monitors V_{IN} and V_{OUT}, drawing V_{IN} current as necessary to keep V_{IN} from rising much beyond 3V above twice V_{OUT}.

The shunt regulator is enabled by connecting the SHUNT pin to the BIAS pin in the circuit board layout. The shunt is disabled by connecting the SHUNT pin to GND.

The shunt regulator dissipates power which must be accounted for in thermal budgeting. Total power dissipation (P_{DSHUNT}) in the LTC3255 with shunt regulator enabled is equal to the input power minus the output power of the LTC3255, or approximately:

$$P_{D(SHUNT)} = P_{IN} - P_{OUT}$$
$$= V_{IN} \bullet I_{IN} - V_{OUT} \bullet I_{OUT}$$
$$\approx (2 \bullet V_{OUT} + 2V) \bullet I_{IN} - V_{OUT} \bullet I_{OUT}$$

where I_{IN} is the time-averaged current being fed into V_{IN} by the current loop, V_{OUT} is the output voltage, and I_{OUT} is the output load current. Notice that the largest power dissipation occurs when output load current is zero. This is because any power fed into V_{IN} must be dissipated in either the load or the LTC3255. If the load is not drawing any current, then the LTC3255 must dissipate all of the input power.

When the shunt regulator is enabled, the LTC3255 charge pump is locked in 2:1 mode. To achieve output regulation, the input current to the part must have sufficient voltage compliance above twice V_{OUT}. The graph in Figure 2 shows the typical minimum compliance required at the V_{IN} pin for correct operation. For $V_{OUT} \leq 5.5V$, a V_{IN} compliance of $2V_{OUT} + 3.5V$ is recommended. For $V_{OUT} > 5.5V$, a V_{IN} compliance of $2V_{OUT} + 4V$ is recommended.

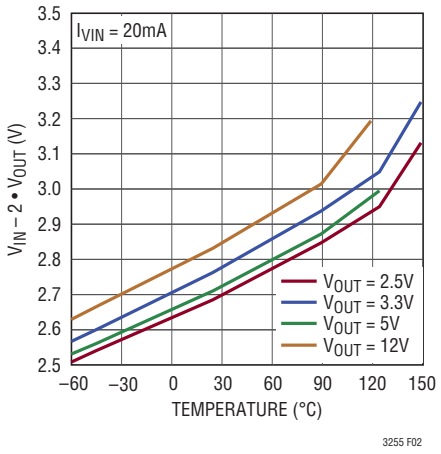


Figure 2. Typical Minimum $V_{IN} - 2 \bullet V_{OUT}$ Compliance Required for Shunt Mode Operation

APPLICATIONS INFORMATION

V_{OUT} Ripple and Capacitor Selection

The type and value of capacitors used with the LTC3255 determine several important parameters such as output ripple and charge pump strength. The value of C_{OUT} directly controls the amount of output ripple for a given load current. Increasing the size of C_{OUT} will reduce the output ripple.

To reduce output noise and ripple, it is suggested that a low ESR (equivalent series resistance < 0.1Ω) ceramic capacitor (10µF or greater) be used for C_{OUT}. Ceramic capacitors typically have exceptionally low ESR which, combined with a tight board layout, should yield excellent performance. Tantalum and aluminum capacitors can be used in parallel with a ceramic capacitor to increase the total capacitance but are not recommended to be used alone because of their high ESR.

V_{IN} Capacitor Selection

The total amount and type of capacitance necessary for input bypassing is very dependent on the impedance of the input power source as well as existing bypassing already on the V_{IN} node. For optimal input noise and ripple reduction, it is recommended that a low ESR ceramic capacitor be used for C_{IN} bypassing. Low ESR will reduce the voltage steps caused by changing input current, while the absolute capacitor value will determine the level of ripple. An electrolytic or tantalum capacitor may be used in parallel with the ceramic capacitor on C_{IN} to increase the total capacitance, but due to the higher ESR, it is not recommended that an electrolytic or tantalum capacitor be used alone for input bypassing. The LTC3255 will operate with capacitors less than 1µF, but depending on the source impedance, input noise can feed through to the output causing degraded performance. For best performance, 1µF or greater total capacitance is suggested for C_{IN}.

Flying Capacitor Selection

The flying capacitor should always be a ceramic type. Polarized capacitors such as tantalum or aluminum electrolytics are not recommended. The flying capacitor controls the strength of the charge pump. In order to achieve the rated output current, it is necessary for the flying capacitor to have at least 0.4µF of capacitance over operating temperature with a bias voltage equal to the programmed V_{OUT} (see Ceramic Capacitor Selection Guidelines). The voltage rating of the ceramic capacitor should be V_{OUT} + 1V or greater.

Ceramic Capacitor Selection Guidelines

Capacitors of different materials lose their capacitance with higher temperature and voltage at different rates. For example, a ceramic capacitor made of X5R or X7R material will retain most of its capacitance from –40°C to 85°C, whereas a Z5U or Y5V style capacitor will lose considerable capacitance over that range (60% to 80% loss typical). Z5U and Y5V capacitors may also have a very strong voltage coefficient, causing them to lose an additional 60% or more of their capacitance when the rated voltage is applied. Therefore, when comparing different capacitors, it is often more appropriate to compare the amount of achievable capacitance for a given case size rather than discussing the specified capacitance value. For example, over rated voltage and temperature conditions, a 4.7µF, 10V, Y5V ceramic capacitor in an 0805 case may not provide any more capacitance than a 1µF, 10V, X5R or X7R available in the same 0805 case. In fact, over bias and temperature range, the 1µF, 10V, X5R or X7R will provide more capacitance than the 4.7µF, 10V, Y5V. The capacitor manufacturer's data sheet should be consulted to determine what value of capacitor is needed to ensure minimum capacitance values are met over operating temperature and bias voltage. Table 1 is a list of ceramic capacitor manufacturers in alphabetical order:

APPLICATIONS INFORMATION

Table 1

CERAMIC CAPACITOR MANUFACTURER	WEBSITE
AVX	www.avxcorp.com
Kemet	www.kemet.com
Murata	www.murata.com
Taiyo Yuden	www.t-yuden.com
TDK	www.tdk.com

Layout Considerations

Due to the high switching frequency and transient currents produced by the LTC3255, careful board layout is necessary for optimal performance. A true ground plane and short connections to all capacitors will optimize performance, reduce noise and ensure proper regulation over all conditions.

When using the LTC3255 with an external resistor divider it is important to minimize any stray capacitance to the FB node. Stray capacitance from FB to C^+ or C^- can degrade performance significantly and should be minimized and/or shielded if necessary.

Thermal Management

The on chip power dissipation in the LTC3255 will cause the junction to ambient temperature to rise at a rate of 40°C/W or more in the MSE package, or 43°C/W or more in the DD package. To reduce the maximum junction temperature, a good thermal connection to the PC board is recommended. Connecting the die paddle (Pin 11) to a large ground plane under the device can reduce the thermal resistance of the package and PC board considerably. Poor board layout and failure to connect the die paddle (Pin 11) to a large ground plane can result in thermal junction to ambient impedance well in excess of 40°C/W (MSE package) or in excess of 43°C/W (DD package). Thermal junction to ambient impedance is specified per JEDEC standard JESD 51-5.

Because of the wide input operating range it is possible to exceed the specified operating junction temperature and even reach thermal shutdown. It is the responsibility of the user of the LTC3255 to calculate worst-case operating conditions (temperature and power) to make sure the LTC3255's specified operating junction temperature is not exceeded for extended periods of time. The 2:1 Step-Down, 1:1 Step-Down, and V_{IN} Shunt Regulator Operation sections provide equations for calculating the power dissipation (P_D) in each mode.

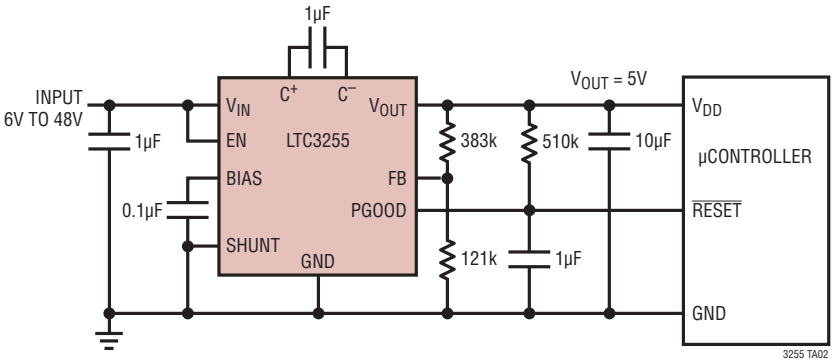
For example, if it is determined that the maximum power dissipation (P_D) is 1.2W under normal operation, then the maximum junction to ambient temperature rise in the MSE package will be:

Junction to Ambient = 1.2W • 40°C/W = 48°C

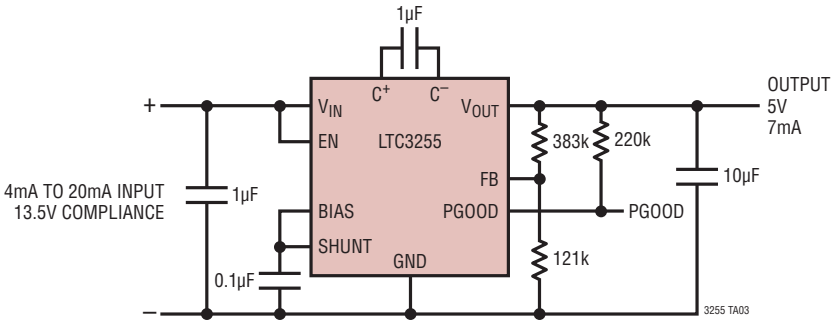
Thus, the ambient temperature under this condition can not exceed 102°C if the junction temperature is to remain below 150°C. For ambient temperatures exceeding roughly 127°C, the device will cycle in and out of the thermal shutdown.

TYPICAL APPLICATIONS

Wide Input Range 5V Microcontroller Supply (with Power-On Reset Delay)



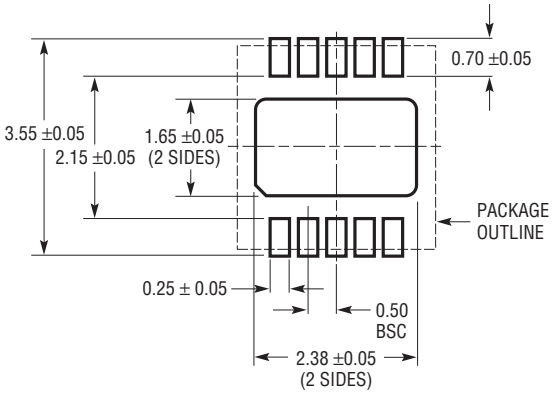
7mA 5V Supply from 4mA to 20mA Current Loop



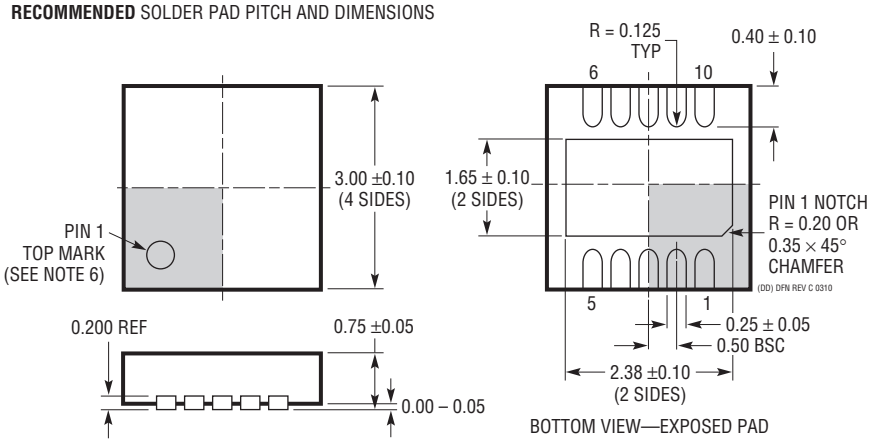
PACKAGE DESCRIPTION

Please refer to http://www.linear.com/designtools/packaging/ for the most recent package drawings.

DD Package
10-Lead Plastic DFN (3mm × 3mm)
(Reference LTC DWG # 05-08-1699 Rev C)



RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS



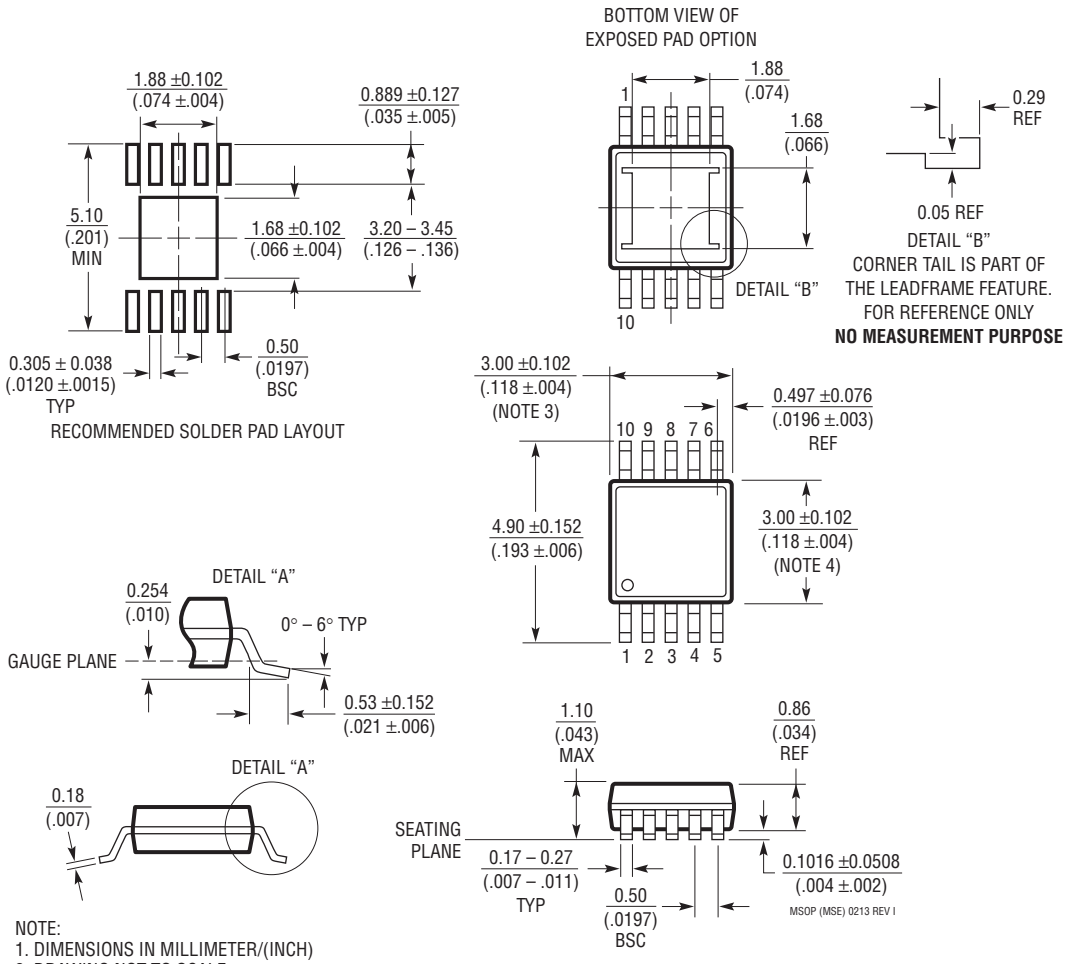
BOTTOM VIEW—EXPOSED PAD

NOTE:
1. DRAWING TO BE MADE A JEDEC PACKAGE OUTLINE M0-229 VARIATION OF (WEED-2).
   CHECK THE LTC WEBSITE DATA SHEET FOR CURRENT STATUS OF VARIATION ASSIGNMENT
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE
   MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE
   TOP AND BOTTOM OF PACKAGE

PACKAGE DESCRIPTION

Please refer to http://www.linear.com/designtools/packaging/ for the most recent package drawings.

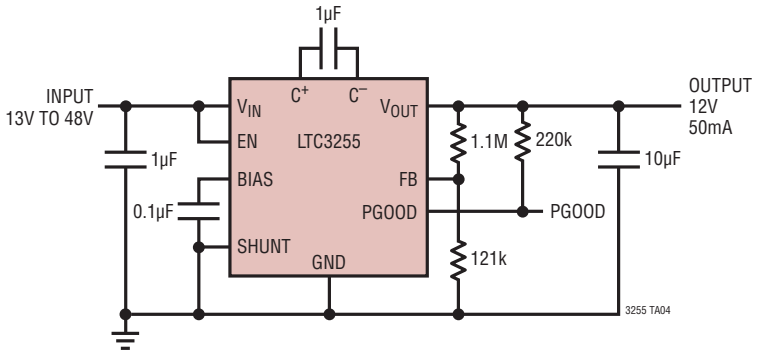
MSE Package
10-Lead Plastic MSOP, Exposed Die Pad
(Reference LTC DWG # 05-08-1664 Rev I)



NOTE:
1. DIMENSIONS IN MILLIMETER/(INCH)
2. DRAWING NOT TO SCALE
3. DIMENSION DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
   MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
4. DIMENSION DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.
   INTERLEAD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
5. LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.102mm (.004") MAX
6. EXPOSED PAD DIMENSION DOES INCLUDE MOLD FLASH. MOLD FLASH ON E-PAD
   SHALL NOT EXCEED 0.254mm (.010") PER SIDE.

TYPICAL APPLICATION

Wide Input Range 12V Supply



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC1751-3.3/LTC1751-5	100mA, 800kHz Regulated Doubler	V_{IN}: 2V to 5V, $V_{OUT(MAX)}$ = 3.3V/5V, I_Q = 20µA, I_{SD} < 2µA, MS8 Package
LTC1983-3/LTC1983-5	100mA, 900kHz Regulated Inverter	V_{IN}: 3.3V to 5.5V, $V_{OUT(MAX)}$ = –3V/–5V, I_Q = 25µA, I_{SD} < 2µA, ThinSOT™ Package
LTC3200-5	100mA, 2MHz Low Noise, Doubler/White LED Driver	V_{IN}: 2.7V to 4.5V, $V_{OUT(MAX)}$ = 5V, I_Q = 3.5mA, I_{SD} < 1µA, ThinSOT Package
LTC3202	125mA, 1.5MHz Low Noise, Fractional White LED Driver	V_{IN}: 2.7V to 4.5V, $V_{OUT(MAX)}$ = 5.5V, I_Q = 2.5mA, I_{SD} < 1µA, DFN, MS Packages
LTC3204-3.3/LTC3204B-3.3 LTC3204-5/LTC3204B-5	Low Noise, Regulated Charge Pumps in (2mm × 2mm) DFN Package	V_{IN}: 1.8V to 4.5V (LTC3204B-3.3), 2.7V to 5.5V (LTC3204B-5), I_Q = 48µA, LTC3204B Version without Burst Mode Operation, 6-Lead (2mm × 2mm) DFN Package
LTC3440	600mA (I_{OUT}) 2MHz Synchronous Buck-Boost DC/DC Converter	95% Efficiency, V_{IN}: 2.5V to 5.5V, $V_{OUT(MIN)}$ = 2.5V, I_Q = 25µA, I_{SD} ≤ 1µA, 10-Lead MS Package
LTC3441	High Current Micropower 1MHz Synchronous Buck-Boost DC/DC Converter	95% Efficiency, V_{IN}: 2.5V to 5.5V, $V_{OUT(MIN)}$ = 2.5V, I_Q = 25µA, I_{SD} ≤ 1µA, DFN Package
LTC3443	High Current Micropower 600kHz Synchronous Buck-Boost DC/DC Converter	96% Efficiency, V_{IN}: 2.4V to 5.5V, $V_{OUT(MIN)}$ = 2.4V, I_Q = 28µA, I_{SD} < 1µA, DFN Package
LTC3240-3.3/ LTC3240-2.5	3.3V/2.5V Step-Up/Step-Down Charge Pump DC/DC Converter	V_{IN}: 1.8V to 5.5V, $V_{OUT(MAX)}$ = 3.3V/2.5V, I_Q = 65µA, I_{SD} < 1µA, (2mm × 2mm) DFN Package
LTC3245	Wide V_{IN} Range Low Noise 250mA Buck-Boost Charge Pump	V_{IN}: 2.7V to 38V, $V_{OUT(MAX)}$ = 5V, I_Q = 20µA, I_{SD} = 4µA, 12-Lead MS and (3mm × 4mm) DFN Packages
LTC3260	Low Noise Dual Supply Inverting Charge Pump	Inverting Charge Pump With Integrated Dual Polarity 50mA LDO Post-Regulated Outputs. V_{IN}: 4.5V to 32V, Charge Pump V_{OUT}: –0.94 • V_{IN}, 100mA
LTC3261	High Voltage, Low Quiescent Current Inverting Charge Pump	V_{IN}: 4.5V to 32V, V_{OUT} = –V_{IN}, I_{OUT} = 100mA, MSOP-12 Package

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